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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/532,103	04/21/2005	Kunio Atago	NIWA	3931

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James C Wray
Suite 300
1493 Chain Bridge Road
McLean, VA 22101

EXAMINER

PHAN, RAYMOND NGAN

ART UNIT	PAPER NUMBER
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2111

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/532,103

Applicant(s)

ATAGO, KUNIO

Examiner

Raymond Phan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 September 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

Part III DETAILED ACTION

Notice to Applicant(s)

1. This action is responsive to the following communications: amendment filed on September 27, 2006
2. This application has been examined. Claims 1-4 are pending.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jewett et al. (US No. 6,263,452) in view of Abbondanzio et al. (US No. 6,931,568).

In regard to claims 1, 4, disclose a control system comprising: a system controller (i.e. first CPU board) comprising a bus arbiter 110 and a non-volatile memory 107 (see figure 4, col.13, lines 10-25); a bus employing a center arbitration method, wherein the single bus arbiter 110 is connected to a plurality of CPUs via a the bus (see col. 14, lines 20-62), from which devices can be detached and to which the detached devices can be attached again as power being supplied (see col. 27, lines 5-48); and a plurality of CPU boards which execute the same processes synchronously (see col. 5, lines 48-65). But Jewett do not disclose having only periodically executed functions and passive functions; wherein: said system controller control the system to continue processes only by periodically executed functions and passive functions of a hardware structure of the system such that when one of said CPU boards on said bus is down while accessing to said non-volatile memory, said system controller assigns the right to use said bus to

other CPU board according to a requirement from said other CPU board; and even if one of the CPU board is down, the system is restored by detaching said down CPU board from said bus and attaching said detached CPU board to said bus again as power for the whole system being supplied. However Abbondanzio et al. disclose management module 120 having only periodically executed functions and passive functions (see col9, line 57 through col. 10, line 48); wherein: said system controller control the system to continue processes only by periodically executed functions and passive functions of a hardware structure of the system such that when one of said CPU boards on said bus is down while accessing to said non-volatile memory, said system controller assigns the right to use said bus to other CPU board according to a requirement from said other CPU board (see figure 6, col. 9, line 57 through col. 10, line 47); and even if one of the CPU board is down, the system is restored by detaching said down CPU board from said bus and attaching said detached CPU board to said bus again as power for the whole system being supplied (see figure 6, col. 10, lines 3-47). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Abbondanzio et al. within the system of Jewett et al. because it would enable the redundant processors and solution not substantially increase the cost and complexity of the system.

In regard to claim 2, Abbondanzio et al. disclose a duplex power source system having a plurality of power sources, wherein: even if one of the CPU boards or power sources is down, the system is restored by detaching said down CPU board or said down power source from said bus and attaching said detached CPU board or said detached power source to said bus again as power for the whole system being supplied (see col. 4, lines 49-65). Therefore, it would have been

obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Abbondanzio et al. within the system of AAPA because it would enable the redundant processors and solution not substantially increase the cost and complexity of the system.

In regard to claim 3, Abbondanzio et al. disclose a duplex IO board system having a plurality of IO boards, wherein: said system controller control the system to continue processes only by periodically executed functions and passive functions of the hardware structure of the system such that when one of said CPU boards or one of said IO boards on said bus is down while accessing to said non-volatile memory, said system controller assigns the right to use said bus to other CPU board or other IO board of said duplex IO board system according to a requirement from said other CPU board or said other IO board; and even if either one of the CPU boards, the IO boards or the power sources is down, the system is restored by detaching said down CPU board, down IO board or down power source from said bus and attaching said detached device to said bus again as power for the whole system being supplied (see figure 3, col. 5, line 64 through col. 6, line 52). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Abbondanzio et al. within the system of AAPA because it would enable the redundant processors and solution not substantially increase the cost and complexity of the system.

Response to Amendment

5. Applicant's amendment and arguments, see on pages 3-7, filed on September 27, 2006, with respect to the rejection of claims 1-4 under 35USC103(a) have been fully considered and are persuasive. Therefore, the

rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Jewett et al.

Conclusion

6. All claims are rejected.
7. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.

Cadambi et al. (US No. 5,261,109) disclose a distributed arbitration method and apparatus for a computer bus using arbitration groups.

Maeda et al. (US No. 5,500,945) disclose an apparatus and method for controlling a system bus of a multiprocessor system.

Pfeifer (US No. 4,805,106) discloses a method and arrangement for ordering of multiprocessor operations in a multiprocessor system with redundant resources.

Klein (US No. 6,108,732) discloses a method for swapping, adding or removing a processor in an operating computer system.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (571) 272-3630. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632 or via e-mail addressed to mark.rinehart@uspto.gov. The fax phone number for this Group is (571) 273-8300.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [raymond.phan@uspto.gov].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through

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Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 central telephone number is (571) 272-2100.

A handwritten signature in black ink, appearing to read 'Raymond Phan', followed by a long horizontal flourish.

Raymond Phan
December 8, 2006